Ozayr Raazi

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Education

University of Waterloo Sept. 2022 – April 2027
Honours Computer Engineering *Waterloo, ON*

- *Relevant Courses*: Digital Hardware Systems, Computer Architecture, Reconfigurable Computing (Graduate-level), Electronic Circuits 2, Real-Time Operating Systems

Skills

Languages: Verilog/SystemVerilog, C, C++, Python, RISC-V, ARMv7, VHDL, Bash
Digital Design: AMD Vivado, Intel Quartus, Verilog-To-Routing (VTR), OpenFPGA, Logisim
PCB/Embedded: Cadence OrCAD X, KiCAD, STM32, Arduino, DediProg, Fusion Digital Power, PowIRCenter
Other: I2C, PMBus, GDB/LLDB, OpenOCD, Git, Linux, Windows, macOS

Experience

Untether AI Jan. 2025 – April 2025
Hardware Engineer (Co-op) *Toronto, ON*

- Designed 4-layer evaluation **Printed Circuit Board** from scratch using Cadence OrCAD X, including component research, schematic diagram, and layout, enabling testing of new Power-Management ICs
- Verified functionality of **40+** AI Accelerator Cards by conducting physical inspections, short checks, performance benchmarks, and neural network correctness tests, while ensuring power/thermal compliance
- Reduced current sensing IC's error to **less than 1%** by sweeping configuration registers and comparing current values measured via **STM32** to adjustable current load's readout, simulating an active board

Untether AI May 2024 – Aug. 2024
Firmware Engineer (Co-op) *Toronto, ON*

- Developed firmware for an **AI Accelerator Card** (PCIe Gen5 x16), enabling key features such as power sequencing, temperature sensing, power monitoring, and fan control, using the **I2C** and **PMBus** protocols
- Brought-up first batch of cards by writing firmware, conducting hardware checks, flashing PMICs, power sequencers and ASICs, and debugging issues, achieving fully booted cards in **under 3 days**
- Researched and proposed switching a voltage rail from single-phase to dual-phase, potentially reducing power loss by **46%** and increasing efficiency by **10%**

Ciena Sept. 2023 – Dec. 2023
Embedded Software Engineer (Co-op) *Ottawa, ON*

- Accelerated iteration and testing of a Segment-Routing module by developing an **event-based** client for simple user interfacing and by configuring CMAKE to enable independent compilation
- Improved error-detection of a TCP-transport library by creating **C++ GoogleTest** unit tests, allowing for send and receive functionalities to be tested concurrently using **multi-threading**
- Increased thread safety of **C code** and protected internal data structures by converting APIs to signal-based

Projects

MVM Engine + Tanh Circuit | *SystemVerilog, AMD Vivado* July 2025

- Implemented a **Matrix-Vector Multiplication** engine from Microsoft's Project Brainwave deep learning accelerator by designing a pipelined dot-product module, accumulator module, and control FSM
- Built a fully pipelined circuit that calculates the Taylor approximation of the hyperbolic tangent function, used for neural network activation, and optimized it to run at **561MHz** on a Pynq-Z1 FPGA using **DSP48E1** blocks

RISC-V CPU + NPU | *Verilog, RISC-V, FPGA* Sept. 2025 – Present

- Building a 5-stage, fully-pipelined, in-order CPU core in **Verilog** based on the RV32I variant of the **RISC-V ISA**
- Designing and implementing a **Neural Processing Unit (NPU)** with dedicated hardware blocks to accelerate key operations in a simple neural network used to predict handwritten digits from the **MNIST** dataset
- Integrating both designs in a **co-processor** package, extending the RISC-V ISA with custom instructions to offload NPU-accelerated operations from the CPU, and aiming to run at maximum frequency on an FPGA